DRAM

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DRAM

- Dynamic Random Access Memory
  - Dynamic:
    - Periodically refresh information in a bit cell.
      - Else it is lost.
  - Small footprint: transistor + capacitor
    - High density memory
      - Cheap.
  - Read complicated
    - Slower than SRAM
DRAM

- First introduced (with a 3T cell) by Intel in 1970.
  - 1kb capacity.
- Classic 1T cell introduced in 1973.
  - 4kb capacity.
DRAM

- DRAM cell
  - Capacitor
  - Transistor
DRAM

- To write a 0
  - Turn bit-line voltage to 0V.
  - Turn word-line voltage to $V_{CC}$
    - Turns access transistor on.
    - Empties charge from capacitor.
  - Turn word-line voltage back to 0V.
To write a 1
- Turn bit-line voltage to $V_{CC}$.
- Turn word-line voltage to $V_{CC}$
  - Turns access transistor on.
  - Charges capacitor.
- Turn word-line voltage back to 0V.
Reading a DRAM cell.
- Capacitor’s common node biased at $V_{CC}/2$
- Cell contains charge of $Q = \pm V_{CC}/2 \cdot C_{Cell}$
- Leak currents slowly remove this charge.

Open the pass transistor:
- Charge distributed over the column line.
- Column line voltage level only changes slightly.
  - $V_{signal} = V_{cell} \cdot C_{cell}/(C_{cell} + C_{line})$
Detect slight voltage change with *Sense Amplifiers.*

Many designs.

Need a reference voltage.
Establish reference voltage.

- Take two column lines
  - One connected to the storage cell.
- Precharge both column lines to exactly the same voltage.
- Connect storage cell to the column line.
- Sense amplifier will pull up / down column line connected to bit.
- Now transfer column line value.
1: Precharge D and D* to exactly the same level.

2: Assert Pass transistor, Change voltage level of D

3: Sense amplifier pulls voltage in D to full level.

4: Close Pass Transistor.
Open DRAM Array
DRAM

- Open DRAM array
  - Reference column line in two separate parts.

- Closed DRAM array
  - Reference column lines close together.
DRAM Read/Write Operation

- DRAM receives row address and column address one after the other.
  - Saves pins for the address bus.

- Signal which part of the address is present:
  - Row Access Strobe (RAS) and
  - Column Access Strobe (CAS) signals.
DRAM Read Operation

- Initially, both RAS* and CAS* are high.
  - All digit lines in the DRAM are **precharged**.
  - All pass transistors are off.
- Apply a valid row address to the address pins of the DRAM.
  - RAS goes low.
  - Latches row address into row address buffer on the falling edge of RAS*.
  - Digit lines are disconnected and allowed to float.
    - But retain the $V_{cc}/2$ voltage level.
- Apply decoded row address to the row line driver.
  - Connects one row of DRAM cells to columns.
  - Lowers or raises voltage in columns by $V_{signal}$. 
DRAM Read Operation

- **Sensing:**
  - Amplification of differential voltage between the column line and the reference line.
  - All digit lines are either at GND or $V_{CC}$ now.

- Assert CAS* to strobe column address into the column address buffer.

- At falling CAS*, decode column address and connect one of the sense amplifiers to data out buffer.

- Deassert RAS*

- Word line goes low.
  - Disconnects DRAM cells in the row from digit lines.
  - All cells in the row have now been charged either to $V_{cc}$ or to GND.
  - They are refreshed.
DRAM Write Operation

1. RAS* and CAS* are high.
   - All digit lines are precharged.

2. Apply row address to row address decoder. RAS* goes low.
   - Enables row decoder.
   - Single word line is asserted.
   - Connects all cells in that row to the digit lines.
DRAM Write Operation

3. Digit lines are slightly pulled up or down.
4. Apply datum. Enable write driver.
5. Valid column address is applied.
   - CAS* goes low.
   - Write driver overdrives sense amplifier selected by address decoder.
6. RAS*, CAS* go high again.
   - Row line goes low and disconnects cells from digit lines.
DRAM Refresh

- DRAM bit cell contents are discharged over time.
- Need to recharge DRAM cells at given times.
- Done by a dummy read.
- One refresh operation refreshes all cells in the same row.
- Uses up some DRAM bandwidth because refresh cannot be done in parallel with other read or write.
DRAM Timing

- After each access, column lines need to be precharged.
- This increases cycle time.
Advanced DRAM Designs

- Page Mode (a.k.a. Burst Mode)
  - Page: contents of bit cells in the same row.
  - After first bit in a page is read, all the other bits are available in the column lines.
    - No need to recharge these column lines if we continue to read in the page.
    - No need to do row address decoding.
  - Initially, use RAS* to strobe in row address.
    - Then continue CAS* to strobe in different column addresses in the same page.
Advanced DRAM Designs

- Extended Data Output (EDO) / Hyperpage Mode
  - In addition, latch the input/output.
  - Longer available than in previous DRAM designs.
  - Allowed for more aggressive timing.
Advanced DRAM Designs

- **Synchronization**
  - Previously: CPU controls access to DRAM.
    - Introduces wait stages.
  - Now: latch input and output latches for data and address, put DRAM under clock control.
    - Less need for signaling between processor and memory.
    - For example, CAS* strobes no longer needed.
      - Page is read successively.
Advanced DRAM Designs

- **Banking**
  - Divide memory in various banks.
  - Try to access different banks in successive accesses.
    - Avoids precharge penalty.

- **Pipelining**
  - Pipelining can speed up the average access time.
    - Pipeline stage 1: latch incoming address.
    - Pipeline stage 2: perform access.
    - Pipeline stage 3: latch output.
Advanced DRAM Designs

- Prefetching
  - Fetch more than a single word at each address cycle.
  - Latch words in an output buffer.
  - Successive requests can usually be dealt with from output buffer.
Advanced DRAM Designs

- **DDR SDRAM**
  - Double data rate synchronized DRAM.
  - 64b data bus.
  - Multiple banks (4)
  - Prefetching
  - Pipelining.
  - Commands are received on rising edge of clock, and data is made available at both rising and falling edge.
    - Hence the name.
Advanced DRAM Designs

- **RAMBUS**
  - Rambus interface
    - Implemented on memory controller and RDRAM
  - Rambus channel
    - 30 high speed, low voltage signals
    - Channel supports up to 32 RDRAM

- **RDRAM**
  - Caching
  - Banking
Chip Layout

- Try to increase capacity of capacitor without increasing footprint.
- Trench capacitor 1970s
- Double stack, fins, spread stacked structures 1990s.
DRAM Trench Capacitor

- Depth of trench increases capacitance of cell.
- Surface footprint small.
- 1980s
DRAM:
Double Stacked Structure
DRAM:
Fin Structure

[Diagram of DRAM fin structure]