1. Suppose you wanted to include a new instruction, `addm`, to the simple five-stage MIPS pipeline. This instruction is similar to `add` except that it accesses memory directly. Explain how you would modify the pipeline to allow this instruction. You may add one or more stages if you feel it is necessary.

12.5

2. Assume the instruction cycle times in the table below. Also, suppose that for the benchmark of interest each instruction type makes up 10% of the total instruction count. How much faster is a multi-cycle implementation than a single-cycle implementation for this particular benchmark?

12.5

It is fine to leave your answer in the form of a fraction (e.g. 5 / 2.5)

Type	**Cycle time**
ALU	6 ns
Load	8 ns
Store	7 ns
Branch	5 ns
Jump	2 ns
Jump and link	6 ns
FP add	20 ns
FP multiply	30 ns
MMX add	12 ns
MMX multiply	20 ns

3. When run on a given system, a program takes 1,000,000 cycles. If the system achieves a CPI of 40, how many instructions were executed when running the program?

5

4. Rewrite the following program fragment to take advantage of register plus immediate addressing mode. Assume that no register values are used outside of the program fragment and that the code fragment will execute on a load-store processor.

12.5

```
ADD r2, r3, #8
LD r4, (r2)
ADD r1, r4, r8
ADD r5, r3, #16
LD r6, (r5)
MUL r7, r1, r6
ADD r9, r3, #24
ST (r9), r7
```

5. Assume it takes 5 ns to read an instruction from memory, 2 ns to decode an instruction, 3 ns to read operands from the register file, 4 ns to perform the computation required by an instruction, and 2 ns to write the result into the register file.

12.5

5 / 5 / 2.5

   a) What is the maximum clock rate of a monolithic processor with these functions?
   b) What is the maximum clock rate of a pipelined processor with these functions?
   c) How many stages are there in the pipeline of part (b) ?

6. You are designing the instruction set for a new machine. The following data summarizes the number of bits required to represent the displacement value for instructions using a displacement addressing mode.

20

5 / 5 / 5 / 5

# bits	% of references
0	25
1	2
2	6
3	13
4	15
5	7
6	10
7	6
8	1
9	1
10	1
11	0
12	0
13	1
14	0
15	12

   a) What is the meaning of a zero-bit immediate?
   b) How would you explain the observation that there are many more references 7 bits or shorter than there are references 8 bits or longer?
   c) What is the average number of bits used in a displacement?
   d) How many bits should be dedicated to encoding displacements in your new instruction set? Justify your choice.

7. Could you use the finite state machine (or something similar to it) that we studied for the multi-cycle CPU to control the simple five-stage pipeline? Why or why not?

10

8. A monolithic single-cycle CPU is redesigned to use an instruction pipeline. Each instruction on the non-pipelined processor takes an average of 4 cycles of 2 nsec each if there are no memory access delays. For the new CPU, the pipeline breaks instructions into 5 stages, each taking one 2.5 nsec cycle if no control, data-dependency or memory delays stall the pipe. The pipeline stages are the same as in the MIPS R2000 pipeline (IF, ID, EX, MEM, WB). Simulation shows the following frequency of execution for instructions and the average number of stall cycles which result from each instruction instance:

15

5 / 2.5 / 2.5 / 5

Instruction Class	Dynamic Frequency	Average Stall Cycles / Instance
Control (branch & jump)	14%	3.00
ALU	60%	1.25
Load	16%	1.25
Other	10%	0.00

50% of the time, after ALU operations or loads, data dependencies cause the very next instruction to stall; sometimes an instruction one later stalls. This gives an average of 1.25 cycles wasted after each ALU instruction and each load. Assume a perfect memory system: every memory access takes only one cycle; there are no stalls during memory access.

a) Without accounting for stalls, how much faster is the pipelined CPU?

b) How much faster is the pipelined CPU once control stalls are considered?

c) How much faster is the pipelined CPU once both control and data stalls are considered?

d) There is a major design flaw in the instruction pipeline that causes many more data dependency stalls than are necessary. In 20 words or fewer, identify the design flaw and briefly describe an easy way to fix it.