CMPUT 229: Computer Organization and Architecture I
Fall 2000–2001, Section A2
Final Exam
Instructor: Paul Lu
(December 13, 2000)

Name: _____ SID: _____

Carefully read all of these instructions and the questions. Good luck!

1. Duration of the examination is 120 minutes.
2. Check that your exam package has 8 pages.
3. Answer all parts of all problems. There are 6 questions worth a total of 100 marks.
4. No books, no notes, and no calculators.
5. You may use the provided MIPS Assembly Language reference pages taken from your textbook. Please return these pages to the instructor at the end of the exam.
6. Be concise, precise, and give clear answers.
7. For the short answers, subjectively better answers will get higher marks. Incorrect or inaccurate statements make an answer subjectively worse.
8. Write all answers on the front of the exam pages and **within the space provided**. You may use the back of these pages for rough work, but it will **not** be marked.
9. If your answer is NOT legible, I cannot mark it.
10. **NOTE**: Here is a decimal, binary and hexadecimal conversion table.

Decimal	Binary	Hexadecimal	Decimal	Binary	Hexadecimal
0	0000	0	8	1000	8
1	0001	1	9	1001	9
2	0010	2	10	1010	A
3	0011	3	11	1011	B
4	0100	4	12	1100	C
5	0101	5	13	1101	D
6	0110	6	14	1110	E
7	0111	7	15	1111	F

Page 2	Page 3	Page 4	Page 5	Page 6	Pages 7–8	
#1	#2	#3	#4	#5	#6	Total
/15	/10	/15	/20	/20	/20	/100

Problem 1 (15 marks in total)

Fill in the blanks. NOTE: Some questions will take more time than other questions.

1. (1 mark) Assuming two's complement representation, the **largest** integer value that can be represented using 5 bits is _____ (in decimal).

2. (1 mark) Assuming two's complement representation, the **smallest** integer value that can be represented using 6 bits is _____ (in decimal).

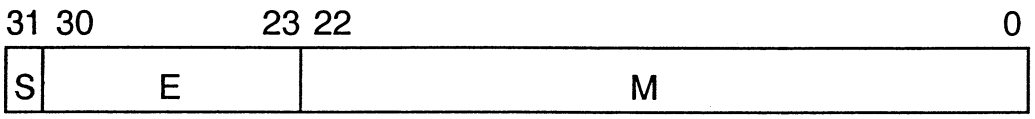
3. (1 mark) The logical AND of 00001110_2 and 10101010_2 is _____ (in binary).

4. (2 marks) Assume a 16-bit address space and a direct-mapped cache. If there are 10 tag bits for each line in the cache and there 4 lines in the entire cache, then the block size must be _____ bytes (in decimal).

5. (2 marks) Assuming two's complement representation and fixed-point numbers, $111110.11_2 + 000000.10_2 =$ _____ (give answer in decimal).

6. (2 marks) Suppose a C program accesses a linked list from the head to the tail and stops. _____ is the kind of locality that is most common in this program.

7. (3 marks) Assume that we are using the IEEE 32-bit floating-point format discussed in class. Recall that the bits are allocated as per:



The decimal value -3.25 is represented as _____ (give answer in hexadecimal) in IEEE 32-bit floating-point.

8. (3 marks) Assume that we are using the IEEE 32-bit floating-point format discussed in class. The 32-bits:

```
0 10000010 00010000000000000000000
```

represents the number _____ (give answer in decimal).

Problem 2 (10 marks in total, 2 marks for each blank)

Consider the following 2-way set-associative cache that already contains some blocks of data from main memory.

Set	Tag	Byte 0	Byte 1	Byte 2	Byte 3
0	1101		[A]		
1	1001				[B]
2	0011			[D]	
	0111			[C]	
3	0111	[E]			

In hexadecimal (and showing the proper number of bytes in an address), what is the **address** of the byte stored at:

1. (2 marks) [A]. The hexadecimal address is _____.

2. (2 marks) [B]. The hexadecimal address is _____.

3. (2 marks) [C]. The hexadecimal address is _____.

4. (2 marks) [D]. The hexadecimal address is _____.

5. (2 marks) [E]. The hexadecimal address is _____.

Problem 3 (15 marks in total, 1 mark for each blank)

You have **direct-mapped** cache capable of holding 32 bytes (plus tag bits). The computer has an address space of 8 bits (0 to 255) and a block size of 2 bytes.

What is the cache behaviour for the memory reference pattern shown (in order) below? Fill in the blanks. **Be careful of the number representation (i.e., binary vs. decimal).**

Assume that the cache is initially empty. If there is a cache hit, specify what kind of locality is responsible for the hit (HINT: There are 2 kinds.). If there is a cache miss, specify what kind of miss it is (i.e., the 3 C's of cache misses). Answer only one (but not both) (a) and (b) for each of the following questions.

1. (3 marks) Address = `0x1F`.

   `Tag` = _____ (in binary). `Line` = _____ (in decimal).

   Answer one of (a) or (b), but not both:

   (a) If a hit, it is due to _____ locality. (b) If a miss, it is a _____ miss.

2. (3 marks) Address = `0xFE`.

   `Tag` = _____ (in binary). `Line` = _____ (in decimal).

   Answer one of (a) or (b), but not both:

   (a) If a hit, it is due to _____ locality. (b) If a miss, it is a _____ miss.

3. (3 marks) Address = `0xB1`.

   `Tag` = _____ (in binary). `Line` = _____ (in decimal).

   Answer one of (a) or (b), but not both:

   (a) If a hit, it is due to _____ locality. (b) If a miss, it is a _____ miss.

4. (3 marks) Address = `0xB0`.

   `Tag` = _____ (in binary). `Line` = _____ (in decimal).

   Answer one of (a) or (b), but not both:

   (a) If a hit, it is due to _____ locality. (b) If a miss, it is a _____ miss.

5. (3 marks) Address = `0xFE`.

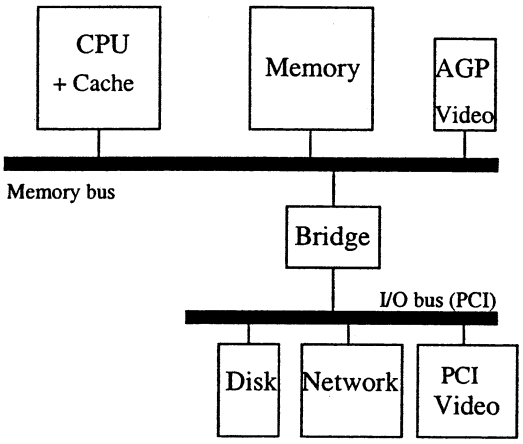
   `Tag` = _____ (in binary). `Line` = _____ (in decimal).

   Answer one of (a) or (b), but not both:

   (a) If a hit, it is due to _____ locality. (b) If a miss, it is a _____ miss.

Problem 4 (20 marks in total, 10 marks for each question)

Short answers (2 or 3 sentences) are expected for the following questions. Keep your answers and explanations **brief** and to the point. Consider the basic computer architecture we studied in class, with some modifications.



1. Suppose that the cache memory at the CPU is no faster than main memory. In other words, the cost of a cache hit is the same as a cache miss. Given this situation, what is a **significant advantage** of having cache memory at all, if any? Explain.

2. Suppose that the CPU is experiencing high cache hit rates **and** the memory bus is busy (i.e., highly utilized). What combination of I/O programming strategies could account for this situation? Explain.

Problem 5 (20 marks in total, 10 marks for each question)
Computer A has 64K of primary cache **and** no secondary cache.

Computer B has 128K of primary cache **and** no secondary cache.

All caches are direct-mapped and all caches have a block size of 256 bytes.

Suppose that the same program (i.e., exact same MIPS executable) is run on Computer A and B, but the program has the exact same **number** of cache misses on both computers.

1. What kind of cache miss (i.e., the 3 C's of cache misses) would be **most** common when executing the program? Explain.

2. A friend suggests that the way to **reduce** the number of cache misses would be to re-design Computer B but with a set-associative cache organization. Do you agree or disagree? Explain.

Problem 6 (20 marks in total, 2 marks for each blank)

The next 2 questions (on 2 pages) refer to the following MIPS assembly language program, which is saved in file `temp.s`. NOTE: Register `$14` is the Exception Program Counter (EPC) Interrupts are turned **off**.

```
        .ktext 0x80000080
        .set noat
        move $k1, $at
        .set at

        sll $t0,$t0,2
        add $t2,$t2,$t1

        mfc0 $k0, $14       # $14 is EPC
        addiu $k0, $k0, 4
        .set noat
        move $at, $k1
        .set at
        rfe
        jr $k0

        .text
        .globl __start
__start:
        li $t5, 0
        li $t6, 5           # Point A
        li $t7, 1
top:
        beq $t5,$t6,exit

        move $t0,$t5
        break 0
        move $t1,$t0
        la $t2,list         # Point B
        break 0

        lw $t0,($t2)        # Point C
        sub $t0,$t0,$t7
        sw $t0,($t2)

        addi $t5,$t5,1
        b top
exit:
        li $v0,10
        syscall             # Good-bye

        .data
list:   .word   0
list1:  .word   2
list2:  .word   4
list3:  .word   6
list4:  .word   8
```

Problem 6 (continued)

Fill in the blanks. NOTE: Use the correct number of hexadecimal digits in your answers!

1. Assume **big-endian** storage. After the above program has been executed with `spim -notrap -file temp.s`, and before it exits, what would be the 32-bit values stored at the memory locations with labels:

   (a) `list` : _____ (in hexadecimal)

   (b) `list1`: _____ (in hexadecimal)

   (c) `list2`: _____ (in hexadecimal)

   (d) `list3`: _____ (in hexadecimal)

   (e) `list4`: _____ (in hexadecimal)

2. Use the addressing mode terminology of Chapter 3 of the textbook or the lecture notes.

   (a) In instruction `li $t6, 5` (labelled `Point A`),

   _____ is the addressing mode of operand `$t6`

   (b) In instruction `li $t6, 5` (labelled `Point A`),

   _____ is the addressing mode of operand `5`

   (c) In instruction `la $t2,list` (labelled `Point B`),

   _____ is the addressing mode of operand `list`

   (d) In instruction `lw $t0,($t2)` (labelled `Point C`),

   _____ is the addressing mode of operand `$t2`

   (e) In instruction `lw $t0,($t2)` (labelled `Point C`),

   _____ is the addressing mode of operand `$t0`